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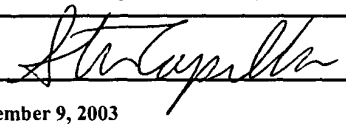
Signature	
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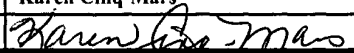
Signature		Date	**September 9, 2003**

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Patentanmeldung Nr. Patent application No. Demande de brevet n°

02368140.6

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Improved dynamic time division multiplexing circuit without a shadow table

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IMPROVED DYNAMIC TIME DIVISION MULTIPLEXING CIRCUIT WITHOUT A SHADOW TABLE

FIELD OF THE INVENTION

The present invention relates to high speed telecommunication systems and more particularly to an improved dynamic time division multiplexing circuit wherein the shadow table which is memory space consuming is no longer required.

BACKGROUND OF THE INVENTION

In telecommunication systems split in several subsystems where data are transmitted on a common media they share, the dynamic Time Division Multiplexing (TDM) access method is extensively used to exchange data between said subsystems. The TDM access method consists in splitting the time in time slots, each one corresponding to a logical channel, i.e. a connection between two subsystems. These logical channels however, have different data throughputs and moreover they are only sporadically active, so that the time slot assignment must be dynamically performed via the use of programmable memories.

FIGS. 1a and 1b illustrate the fundamentals of the TDM access method. Now turning to FIG. 1a, there are shown six subsystems labeled A to F, that exchange information via a bi-directional common media referenced 10 (e.g. two transmission wires) at different times. For instance, the double arrow that links subsystems A and C illustrates a connection corresponding to a logical channel for full duplex

data transmission therebetween at a given time and for a determined duration, to subsequently allow the other pairs of subsystems to communicate between them as suggested by the other double arrows. The maximum number of possible bi-directional logical connections is given by factorial 5 (5!), i.e. 120. In fact, the number of logical connections that is required in reality is much limited. As apparent in FIG. 1a, three double arrows are represented to illustrate full duplex connections only between subsystems A-C, B-E and D-F.

FIG. 1b shows an example of the assignment of the eight data bit positions labeled Bit1 to Bit8 (and more generally of n bit positions) of a TDM frame to three different logical channels X, Y and Z at a given time. These three logical channels which are distinguished one from the another by their respective identifier: LC X, LC Y and LC Z, correspond to the full duplex connections between subsystems A-C, B-E and D-F in the example mentioned above. More generally, these identifiers can be understood as represented by a number coded on p bits, associated to any logical channel/connection between two subsystems. As apparent in FIG. 1b, two bit positions (Bit1-Bit2) are assigned to LC X, four bit positions (Bit3-Bit4-Bit5-Bit6) to LC Y and finally, two bit positions (Bit7-Bit8) to LC Z. This assignment thus defines the corresponding time allocation for each logical channel, three time slots in this example, labeled TimeslotX, TimeslotY and TimeslotZ respectively. A Time Slot Assignment (TSA) table referenced 11, describing the different time slots by specifying which logical channel each data bit position belongs to, can be then set up. Therefore, in the above described example, wherein the 8-bit TDM frame is composed of three time slots of different sizes, the common media 10 that transports the serial data bits can be seen as composed of three logical channels of different throughputs (the throughput being proportional to the number of data bits).

Because, the content of the TSA table is time dependent, the logical channel that is assigned to each of the TDM frame data bit position is variable. The data bits that fill the eight positions for each TDM frame, are stored in dedicated First-In First-Out (FIFO) memories, each FIFO storing the data bits belonging to a determined logical channel. In other words, the content of each data bit position in the data stream transported on the common media 10 is determined by the logical channel assigned thereto, and this assignment dynamically changes.

A conventional technique of the prior art consists to provide a dynamic time slot assignment wherein two TSA tables are used at a given time, one being the active and the other the shadow table. While the active table is exploited by the time slot assignor, the shadow table may be updated by the application software to describe a new time slot assignment. Next, when appropriate, the tables are then swapped so that the shadow table is used as the active one and vice versa. FIG. 2 illustrates a standard dynamic time division multiplexing circuit referenced 20 that implements such a conventional approach.

Now turning to FIG. 2, the active TSA table stored in memory block 21-1 contains a determined set of logical channel identifiers, e.g. LC X, LC Y and LC Z to remain consistent with the example described above by reference to FIG. 1b, while the shadow TSA table stored in memory block 21-2 contains another set thereof. The zero ("0") value means that the corresponding data bit is not assigned to any logical channel. Each memory block has n fields. The two TSA tables stored in memory blocks 21-1 and 21-2 can be swapped, written and read by a computer (or a microprocessor) under the control of an adequate application software as standard. These operations are performed through demultiplexer 22 which interfaces the computer and the memory blocks 21-1/21-2 via

bi-directional buses 23 and 24a/24b respectively. On the other hand, the memory blocks 21-1 and 21-2 are connected to multiplexer 25 via buses 26a and 26b respectively, and in turn, multiplexer 25 is connected to the time slot assignor 27 via output bus 28. The time slot assignor 27 basically consists of a multiplexer driven by said output bus 28, i.e. the content of memory blocks 21-1 and 21-2 (only one can be accessed for a read operation at a given time) and a counter (not shown). The multiplexer is fed by a plurality of FIFOs and its output is the common media 10. The role of the time assignor 27 is to control the transmission of data bits on the common media 10 or the reception of data bits to load the FIFOs.

Assuming the TSA table stored in memory block 21-1 is made active and is exploited by the time slot assignor, the other one, stored in memory block 21-2, becomes the shadow TSA table and can be updated by the computer. As apparent in FIG. 2, while the time slot assignor reads the active TSA table to get the current time slot assignment (via the data path illustrated by gray arrow 29a), the computer edits the shadow TSA table for data updating (via the data path illustrated by double gray arrow 29b). The role of the computer is not to select which TSA table must be active but rather to determine the time when a swapping operation is necessary. In case of full duplex serial transmission, two circuits 20 are necessary in reality, the first circuit controls the transmission of data bits from the FIFOs to the common media 10 for subsequent processing and the second one controls the selective loading of data bits transported on the common media 10 in their respective FIFOs.

This approach is very flexible, as it allows any kind of modification between the old and new time slot assignments, but it has the important drawback to require two memory blocks, typically SRAMs, to store the TSA tables which may be

very large, consuming thereby a huge memory space therein. To date, it is classic to transmit data bits at 8.0192 Mbit/s, within a 125 µs time frame. In this case, a pattern is comprised of n = 1024 bits (instead of 8 bits in the above example depicted in FIG. 1b), and thus two TSA tables, each one with 1024 entries, are required. On the other hand, in a typical application to telephony, it is also standard practice to have up to N = 256 logical channels sharing the same common media 10, so that p = 8 bits are required per logical channel to code its identifier. Therefore, still in this particular example, the memory space that is required to store either active or shadow TSA table would be nxp bits, i.e. 1024x8 bits.

With regards to the above described approach which basically requires to have two SRAM memory blocks (one dedicated to store the active TSA table, the other to store the shadow TSA table), one demultiplexer circuit and one multiplexer circuit, the present invention aims to describe a new way which is much more efficient in most applications as it drastically decreases the amount of memory space that is required, and obviates the use of said demultiplexer/multiplexer circuits.

SUMMARY OF THE INVENTION

It is therefore a primary object of the present invention to provide an improved dynamic time division multiplexing (TDM) circuit wherein the SRAM memory block storing the shadow table is no longer required and is replaced by simple register for a significant saving of the memory space.

It is another object of the present invention to provide an improved dynamic time division multiplexing circuit wherein the need of demultiplexer/multiplexer circuits is obviated for circuit design simplification and silicon space saving when the TDM circuit is integrated in a silicon chip.

According to the present invention there is described an improved dynamic time division multiplexing circuit to be inserted in a telecommunication system split in a plurality of subsystems adapted to exchange serial data bits therebetween. Said serial data bits are arranged in n-bit frames according to the dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position of said frame is associated either one among N logical channels or a null value wherein N is the maximum number of logical channels that can be simultaneously opened. In addition, to each logical channel is associated an identifier coded on p bits. Said improved circuit first comprises first data storage means comprising a nxp memory block to store the time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots and second data storage means comprising a Nx1 register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value. Said first and second data storage means are connected to input bus means for inputting the logical channel identifiers into said first data storage means and the value of the status bits in said second data storage means from a computer or an application software. Finally, it further comprises logic circuit means connected to said first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" to an output bus means for subsequent processing by a time slot assignor.

The novel features believed to be characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may be best understood by reference to the following

detailed description of an illustrated preferred embodiment to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a shows a plurality of subsystems sharing a bi-directional common media that is used to provide the physical support for full duplex data exchange between three determined pairs thereof for a given bit frame/pattern.

FIG. 1b schematically shows a Time Slot Assignment (TSA) table which describes the different time slots by specifying which logical channel/connection each bit of the pattern belongs to, according to the dynamic Time Division Multiplexing (TDM) access method.

FIG. 2 shows a conventional dynamic time division multiplexing circuit to dynamically provide a time slot assignment that is comprised of two memory blocks to store the active and shadow TSA tables, a demultiplexer fed by the application software stored in a computer and a multiplexer connected to the time slot assignor.

FIG. 3 shows the improved dynamic time division multiplexing circuit according to the present invention wherein the memory block storing the shadow TSA table is no longer required, a simple register being used instead for significant memory space saving.

FIG. 4 schematically shows a typical implementation of the logic circuit illustrated in FIG. 3.

FIG. 5 shows the different steps to make the FIG. 3 circuit operative and for its update (opening/closing of a new logical channel, ...).

DESCRIPTION OF A PREFERRED EMBODIMENT

In practice, the flexibility offered by the conventional circuit of FIG. 2 is not needed in most applications. The only modifications which need to be applied in real time to the time slot assignment consist in the opening/creation or the closing/deletion of logical channels as exchanges between subsystems appear or disappear. Notwithstanding, this level of flexibility which is really required by some applications can be reached by the improved dynamic TDM circuit of the present invention. The memory block storing the shadow TSA table and the demultiplexer/multiplexer circuits are no longer required. Now, according to the present invention, only one memory block to store the TSA table, a register and a very simple logic circuitry need to be implemented in hardware. A specific initialization and update procedure adapted to said improved dynamic TDM circuit will be also described hereinbelow.

Considering FIG. 3, the improved dynamic TDM circuit referenced 30 now consists of a single memory block 31 (typically a SRAM) to store the TSA table records, a register 32 and a logic circuit 33. The memory block 31 still has n memory fields referenced Bit1 to Bitn, assuming n-bit TDM frames are processed, to store the logical channel identifiers still coded on p bits. The role of register 32 is to store one "status" bit per logical channel. Assuming that the maximum number of logical channels that can be simultaneously opened is represented by N, register 32 thus has N fields to store the status bits with a granularity of one bit. These fields are referenced LC 1 to LC N in FIG. 3, i.e. By the logical channel identifier associated thereto for the sake of simplicity. Using the same assumptions as described above, the memory space that is now required is only 1024x8 bits (in memory block 31) and 256x1 bits (in register 32) ensuring thereby a significant memory space saving as a whole. Note that this advantage increases as the transmission rate increases. When a TSA table record specifies a logical channel

identifier for which the status bit in the register 32 associated thereto is "0", the corresponding data bit is considered as being not assigned to any logical channel. In this case, the computer can update this record without any impact for the time slot assignor. If the associated status bit in the register 32 equals "1", then the corresponding data bit is considered as being assigned to the logical channel specified in the TSA table record. The memory 31 and the register 32 are accessed by the application software stored in the computer via bi-directional bus 34. On the other hand, they are connected to logic circuit 33 via unidirectional buses 35 and 36 respectively. Logic circuit 33 is coupled to the time slot assignor via unidirectional bus 37. As apparent in FIG. 3, as far as logical channel identifier LC X is concerned, the "1" that is associated thereto in register 32, indicates that this logical channel is assigned. Let us assume that improved TDM circuit 30 controls the transmission of data bits and that Bit1 is the current bit position, the 8 bits coding logical channel identifier LC X are sent to the time slot assignor, which in turn, will output the first data bit from the FIFO dedicated to store the data bits assigned to LC X. The same operation is repeated for Bit2, so that two data bits assigned to logical channel X will be transmitted on the common media 10 as the first time slot. As apparent in FIG. 3, the demultiplexer 22 and the multiplexer 25 of the FIG. 2 circuit are no longer required at the cost of logic circuit 33 which can be physically implemented very simply. In essence, this logic circuit 33 propagates the logical channel identifier specified in the current TSA table record to the time slot assignor if its associated status bit is set to "1" in the register 32. The time slot assignor then knows from which FIFO, the current data bit must be extracted. In the contrary, if the associated status bit is set to "0" in the register 32, the logic circuit 33 propagates a null logical channel identifier, which means "unassigned". In this case, a default value is sent in lieu of a data bit, which is

recognized by the receiver (in case of a transmission). As matter of fact, assigning a data bit to a deactivated channel is like unassigning it.

FIG. 4 is a schematic implementation of the logic circuit 33 shown in FIG. 3. Now turning to FIG. 4, logic circuit 33 basically consists of a logic block 41 made of p two-way AND gates 42-1 to 42-p and a N-input selector 43. Selector 43 receives the N bits stored in register 32 as inputs via bus 36 and is controlled by the p bits of bus 35 to select one among said N inputs. Each of the p bits of bus 35 are also applied to one input of AND gates 42-1 to 42-p which receive the bit generated by the selector 43 on their other input. The p bits output by AND gates 42-1 to 42-p are bundled to form bus 37.

Operation of logic circuit 33 can be understood as follows. The TSA table stored in memory block 31 is read in sequence from the first field (Bit1) to the last one (Bitn) under the control of a specific serial clock. This operation is performed cyclically. Let us assume for example that the first TSA table record, i.e. LC X, is read. This p-bit binary word becomes available on bus 35 and each one of the p bits is applied on the first input of AND gates 42-1 to 42-p. Simultaneously, once decoded internally in selector 43, this binary word also selects the associated status bit at field LC X, which in the example depicted in FIG. 3 is equal to "1". This value is applied to each second input of said AND gates, enabling them to transmit said first record LC X to the time slot assignor via bus 37. If the associated status bit stored in register 32 would have been a "0" instead of a "1" (see for instance LC Y), the TSA table record would not have been sent to the time slot assignor, because the AND gates would have been disabled.

The essential steps of the procedure to update the TSA table stored in memory block 31 and the status bit held in register

32 shown in FIG. 3 will be now described in details by reference to FIG. 5. Now turning to FIG. 5, before any TSA table updating is performed, a preliminary step of initialization is required (box 51).

TSA table initialization (51)

After a global RESET operation, performed for instance at the chip level, register 32 is set to all-zeroes, so that all the logical channels are deactivated. This means that whatever the content of the TSA table, all the data bits are considered as being assigned to none logical channel, i.e. unassigned, and the common media 10 is continuously driven to a default value. At that time, the application software initializes all the fields of the TSA table to zero if this has not already been done by the RESET operation.

Let us assume now that we want to open a new logical channel/connection, two steps are then necessary, one to allocate bits to that logical channel (box 52) and the other to activate it (box 53).

Channel allocation (52)

When the application software stored in the computer wishes to open a new logical channel, for example logical channel X bearing identifier LC X, first of all, it needs to allocate data bits to this logical channel. To that end, it makes sure that logical channel X is deactivated via its associated status bit held in register 32. Then, it updates the appropriate number of unassigned TSA table records to now refer to logical channel X, by setting fields in memory block 31 to its identifier LC X. It should be noted that this modification can be done dynamically because assigning a data bit to a deactivated channel is like unassigning the data bit. So, although this operation changes the memory block 31

content, the time slot assignment seen by the time slot assignor appears unchanged.

Channel activation (53)

When the application software decides to activate logical channel LC X, it enables it by setting to one its associated status bit in register 32. The time slot assignor then detects that data bits are assigned to an activated logical channel and consequently determines the data bits of the corresponding time slot as belonging to LC X. The atomic nature of this channel activation (i.e. indivisible and very brief), makes the whole operation (allocation and activation) to also appear atomic for the time slot assignor even if several memory accesses were required to open this new logical channel.

Let us assume now that after logical channel X has been opened as described above, it is needed to create a new connection. This operation is performed through the steps of new channel allocation (box 54) and new channel activation (box 55).

New channel allocation (54)

When the software needs to open a new logical channel, for example logical channel LC Y, it first makes sure that LC Y is deactivated via register 32. Then, it updates unassigned TSA table records to refer to LC Y. This operation has no effect on the already assigned ones, so that the active LC X is not impacted. This modification can be done dynamically because, as said above, assigning a data bit to a deactivated channel is like unassigning it. Therefore, although this operation changes the content of memory block 31, the time slot assignment seen by the time slot assignor appears unchanged.

New channel activation (55)

After the new channel allocation step has been completed, the application software activates the new logical channel, Y in the present case, via the register 32. This causes the time slot assignor to determine the data bits of that time slot as belonging to LC Y to start driving the common media 10. Again, in view of the atomic nature of this channel activation, the whole operation (allocation and activation) also appears atomic for the time slot assignor even if several memory accesses were required to open this new logical channel.

The last case to be studied consists in the closing operation to delete a connection while other (s) are let operative. Sill in this case, two steps are necessary to deactivate the logical channel corresponding to that connection (56) and deallocate this logical channel (57).

Channel deactivation (56)

When the application software decides that a logical channel, X in this example, is no longer needed and should be closed, it deactivates LC X via register 32. Since that time, all the corresponding TSA table records which refer to LC X are simultaneously seen as being unassigned (atomic operation). The time slot assignor consequently determines the data bits of the time slot as being unassigned. In the transmission mode, the time slot assignor drives the default value in the common media 10 during the corresponding time slot, while in the reception mode the data bits are ignored.

Channel deallocation (57)

Once the logical channel is deactivated, which is checkable via register 32, the application software can free the corresponding data bits by setting their logical channel identifier fields to zero. This modification can be done dynamically because, as said above, unassigning a data bit is

like assigning it to a deactivated channel. Therefore, although this operation changes the content of memory block 31, the time slot assignment seen by the time slot assignor appears unchanged.

In summary, although there is only one TSA table instead of two, usually referred to as the active and shadow tables, the application software can dynamically change the time slot assignment, in particular, it can open or close connections while other ones are running. The opening/closing operations appear also as being atomic for the time slot assignor despite they required several memory accesses for the application software. This leads to big savings in term of memory cell count as the shadow TSA table may be very large, as its size depends of both the length n of the TDM frame and the number p of bits necessary to code the number N. The latter is the maximum number of logical channels that can be simultaneously opened. The only constraint is that register 32 must contain the status (activated/deactivated) of all the logical channels and to implement a very simple logic circuit to propagate or not the logical channel identifier.

While the invention has been particularly described with respect to a preferred embodiment thereof it should be understood by one skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. In a telecommunication system split in a plurality of subsystems adapted to exchange serial data bits arranged in n-bit frames according to the dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position (Bit1 to Bitn) of said frame is associated either one among N logical channels or a null value, N being the maximum number of logical channels (..., X, ...) that can be simultaneously opened and wherein to each logical channel (X) is associated an identifier (LC X) coded on p bits, the improvement comprising:

first data storage means (31) comprising a nxp memory block to store the time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots (TimeslotX, ...);

second data storage means (32) comprising a Nx1 register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value;

input bus means (34) for inputting the logical channel identifiers into said first data storage means and the value of the status bits in said second data storage means from a computer or an application software; and,

logic circuit means (33) connected to said first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" to an output bus means (37) for subsequent processing by a time slot assignor (27).

2. The telecommunication system according to claim 1 wherein the null value corresponds to a bit position to which none logical channel is assigned.

ABSTRACT

IMPROVED DYNAMIC TIME DIVISION MULTIPLEXING CIRCUIT WITHOUT A SHADOW TABLE

The present invention relates to a telecommunication system split in a plurality of subsystems that is adapted to exchange n-bit frames therebetween according to the dynamic time division multiplexing (TDM) access method. According to that method, the time is split in time slots, each one corresponding to one among N logical channels, wherein N is the maximum number of logical channels that can be simultaneously opened. To each logical channel (X, ...) is associated an identifier (LC X, ...) coded on p bits. In accordance with the present invention, the improved circuit (30) first comprises a nxp memory block (31) to store the time slot assignment (TSA) table which describes the different time slot assignments by specifying which logical channel each bit position of the n-bit TDM frame (Bit1 to Bitn) it belongs to. It further comprises a register (32) having N fields with a granularity of one bit, each bit indicates the status of the corresponding logical channel associated thereto: "assigned" when it has a first value or "unassigned" when it has another value. Finally, it comprises a logic circuit (33) connected to said memory block and register that enables or disables the transmission of the logical channel identifier to a time slot assignor depending on the status bit value.

FIG. 3

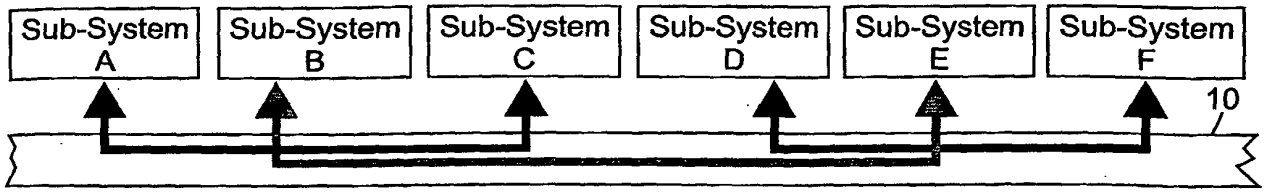


FIG. 1a (Prior Art)

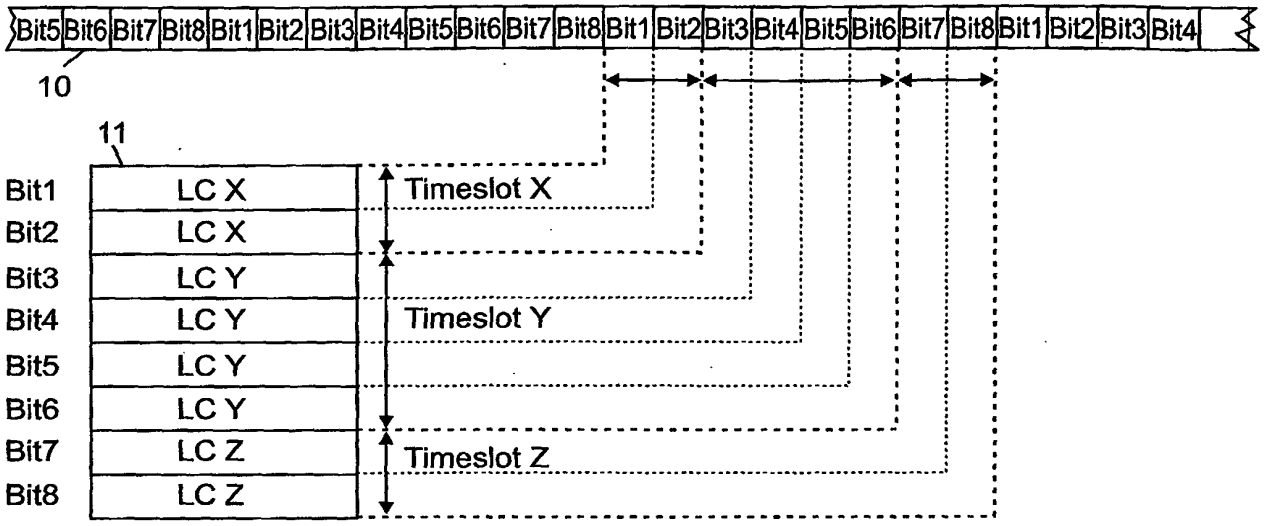


FIG. 1b (Prior Art)

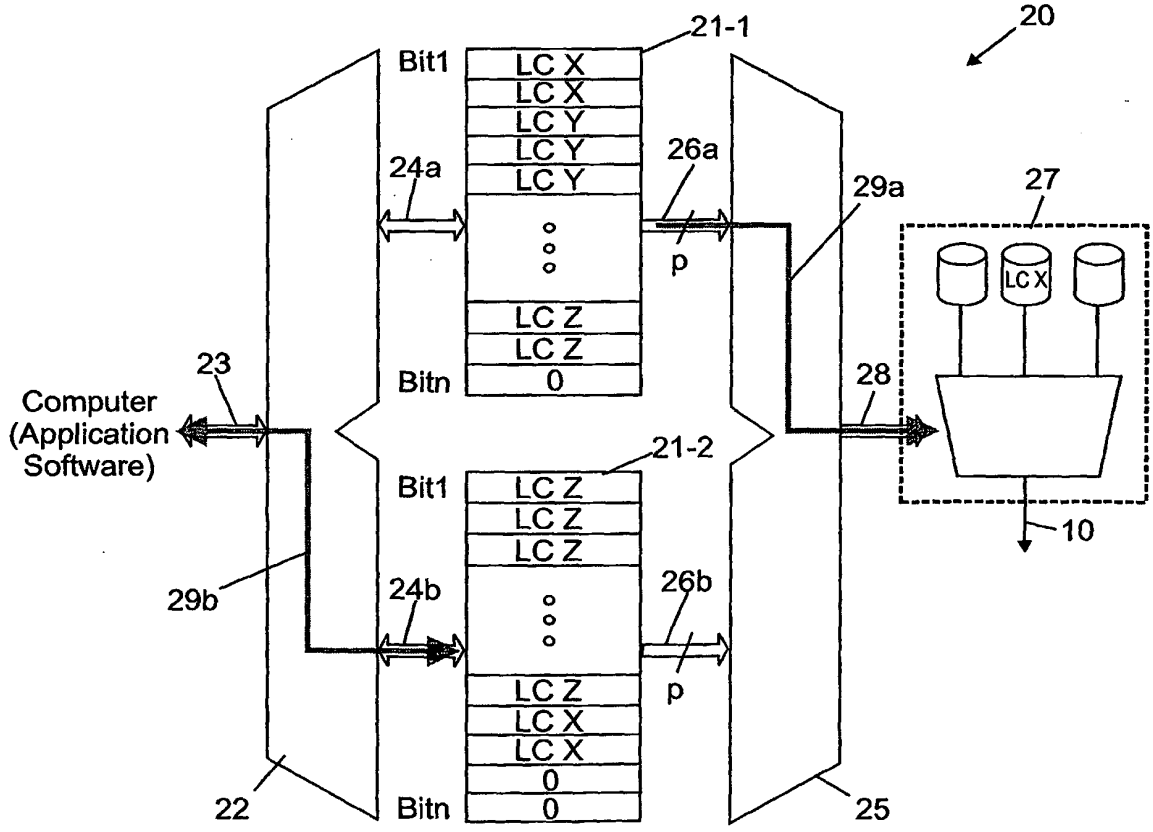
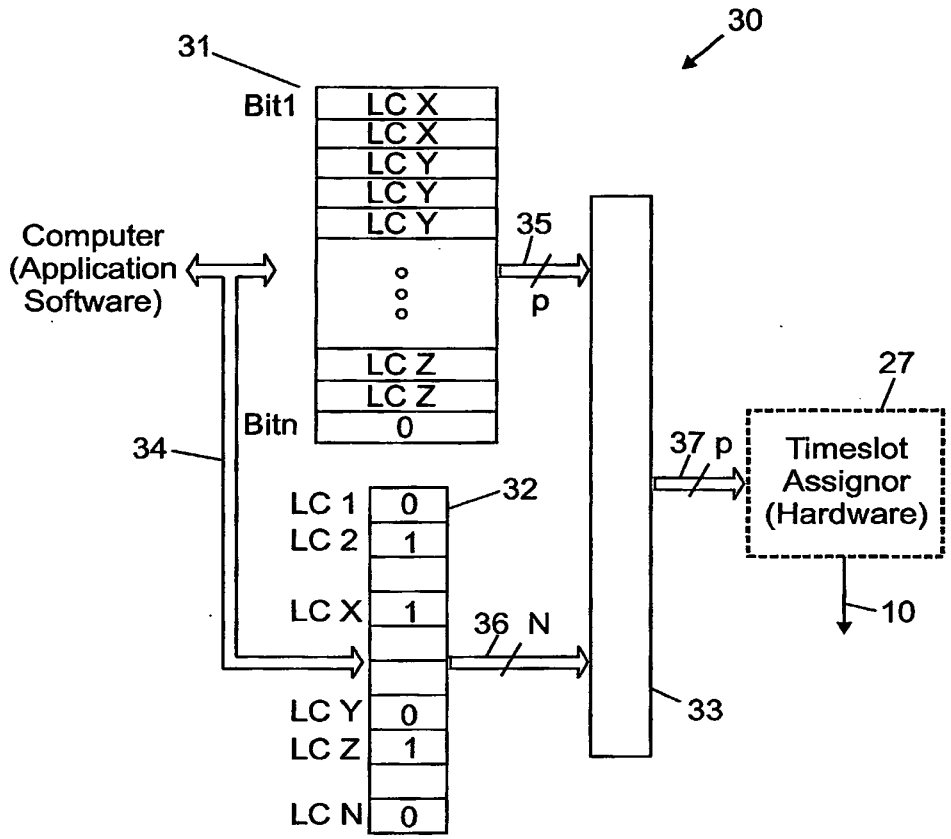


FIG. 2 (Prior Art)


30
31
Bit1
LC X
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LC Y
LC Z
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Computer
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35
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27
Timeslot
Assignor
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10
37 p
34
LC 1
LC 2
LC X
LC Y
LC Z
LC N
0
1
1
0
1
0
32
36 N
33

FIG. 3

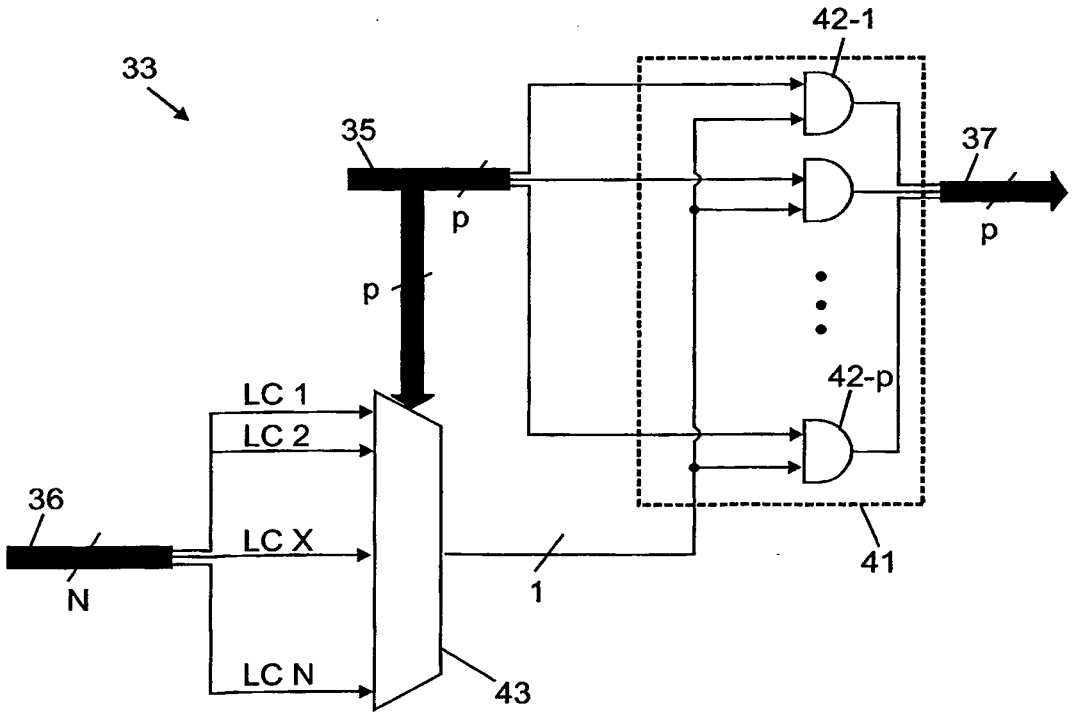
33
42-1
35
p
37
p
p
42-p
LC 1
LC 2
36
LC X
N
1
41
LC N
43

FIG. 4

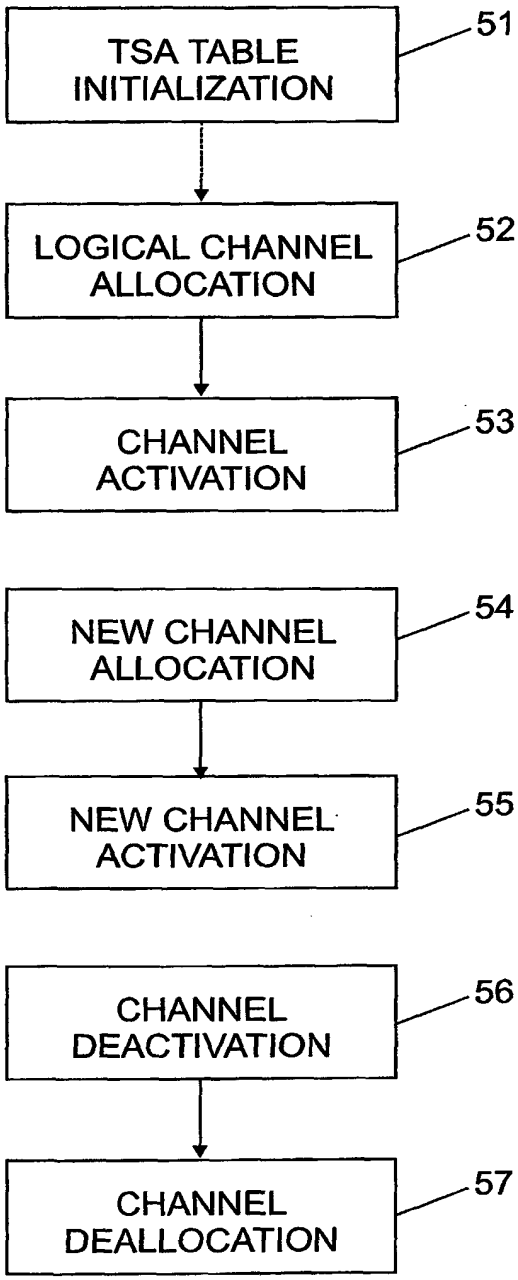
TSA TABLE INITIALIZATION
51
LOGICAL CHANNEL ALLOCATION
52
CHANNEL ACTIVATION
53
NEW CHANNEL ALLOCATION
54
NEW CHANNEL ACTIVATION
55
CHANNEL DEACTIVATION
56
CHANNEL DEALLOCATION
57

FIG. 5